

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figure11" and substitute --Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

**IN THE CLAIMS:**

Kindly cancel claims 1-150, without prejudice.

Kindly add the following claims:

1 -- 151. A method of controlling a memory device, wherein the  
2 memory device includes a plurality of memory cells, the method of  
3 controlling the memory device comprises:

4 providing first block size information to the memory device,  
5 wherein the first block size information defines a first amount of  
6 data to be input by the memory device in response to a write  
7 request; and

8 issuing a first write request to the memory device, wherein in  
9 response to the first write request the memory device inputs the  
10 first amount of data corresponding to the first block size  
11 information.

1 152. The method of claim 151 wherein the memory device inputs  
2 the first amount of data synchronously with respect to an external  
3 clock signal.

1 153. The method of claim 151 further including:  
2 providing second block size information to the memory device,  
3 wherein the second block size information defines a second amount  
4 of data to be input by the memory device in response to a write  
5 request; and  
6 issuing the second write request to the memory device, wherein  
7 in response to the second write request, the memory device inputs  
8 the amount of data corresponding to the second block size  
9 information.

1 154. The method of claim 151 wherein the first block size  
2 information and the first write request are included in a request  
3 packet.

1 155. The method of claim 154 wherein the first block size  
2 information and the first write request are included in the same  
3 request packet.

1 156. The method of claim 151 further including providing  
2 the amount of data corresponding to the first block size  
3 information to the memory device.

1 157. The method of claim 156 wherein the data is provided to  
2 the memory device after a delay time transpires.

1 158. The method of claim 156 wherein the delay time is  
2 representative of a number of clock cycles of a clock signal.

1 159. The method of claim 151 wherein the first block size  
2 information is a binary representation of the amount of data to be  
3 input in response to the first write request.

1 160. The method of claim 151 wherein the first amount of data  
2 corresponding to the first block size information is input  
3 synchronously during a plurality of clock cycles of the external  
4 clock signal.

1 161. A method of operation of a memory device, wherein the  
2 memory device includes a plurality of memory cells, the method of  
3 operation of the memory device comprises:

4 receiving first block size information from a bus controller,  
5 wherein the first block size information defines a first amount of  
6 data to be input by the memory device in response to a write  
7 request;

8 receiving a first write request from the bus controller; and  
9 inputting the first amount of data corresponding to the first  
10 block size information in response to the first write request.

1 162. The method of claim 161 wherein the data corresponding to  
2 the first block size information is sampled synchronously with  
3 respect to the external clock signal.

1 163. The method of claim 161 further including:  
2 receiving second block size information, wherein the second  
3 block size information defines a second amount of data to be input  
4 in response to a second write request;  
5 receiving a second write request from the bus controller; and  
6 inputting the amount of data corresponding to the second block  
7 size information, in response to the second write request.

1 ~~164.~~ The method of claim ~~161~~ wherein the first block size  
2 information and the first write request are included in a request  
3 packet.

1 ~~165.~~ The method of claim ~~164~~ wherein the first block size  
2 information and the first write request are included in the same  
3 request packet.

1 ~~166.~~ The method of claim ~~161~~ wherein the first block size  
2 information is a binary representation of the first amount of data  
3 to be input in response to the first write request.

1 ~~167.~~ The method of claim ~~161~~ wherein the first amount of data  
2 corresponding to the first block size information is input

3 synchronously during a plurality of clock cycles of an external  
4 clock signal.

1 168. The method of claim 161 further including generating an  
2 internal clock signal using a delay locked loop and an external  
3 clock signal wherein the first amount of data corresponding to the  
4 first block size information is input synchronously with respect to  
5 the internal clock signal.

1 169. The method of claim 161 further including generating  
2 first and second internal clock signals using clock generation  
3 circuitry and an external clock signal wherein the first amount of  
4 data corresponding to the first block size information is input  
5 synchronously with respect to the first and second internal clock  
6 signals.

1 170. The method of claim 169 wherein the first and second  
2 internal clock signals are generated by a delay lock loop.

1 171. A method of operation of an integrated circuit, wherein  
2 the integrated circuit includes a memory array having a plurality  
3 of memory cells, the method of operation comprises:

4 receiving block size information, wherein the block size  
5 information defines a first amount of data to be input ~~from a bus~~  
6 in response to a write request;

7 receiving a first write request; and